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10/007,332	11/08/2001	Andrew Marshall	TI-31484	3238

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,332	MARSHALL	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11/8/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 14 is objected to because of the following informalities: claim 14 is a duplicate of claim 12 and does not further limit the independent claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 6 states that a "physical connection of metallic material...does not carry current during normal operation of said circuit stage." The specification, which is enabling for metallic material to couple devices, does not adequately disclose or even mention that the metallic material does not carry current during normal operation. One of ordinary skill in the art would assume that a metal connected between two active devices would carry a current. Because it is not understood how the metal material

"does not carry current", for the purposes of a prior art rejection the examiner will interpret the limitation to mean that there is a physical connection of metallic material which provides thermal conduction between the respective bodies of the pair of transistors. This interpretation will remain until further evidence is shown in the specification that such a configuration is possible.

Claim 10 states that bodies of matched transistors "are not tied to any fixed potential." The specification is not enabling for the limitation because it does not mention that the bodies are not tied to any fixed potential. It is shown in the specification that the bodies are totally isolated from other components or devices however it still does not mean that there can't be a potential tied to the body. It seems that if a source or drain is tied to a fixed potential, then the body of the transistor is also tied to a fixed potential. It is unclear how this is possible since there is no mention of such a limitation. For purpose of a prior art rejection, the examiner will interpret the limitation to mean that the body is isolated from other components. This interpretation will remain until evidence is shown in the specification that such a configuration is possible.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 5, 16-19, and claims 6 and 9, as far as understood, are rejected under 35 U.S.C. 102(a) as being anticipated by Flaker et al. (US 6,133,608).

In re claim 1, Flaker et al. shows (fig. 10B or 20) an integrated circuit semiconductor-on-insulator structure, comprising a pair of matched transistors, in a circuit stage which requires matched behavior of said pair (col. 7, lines 15-24) and a physical connection of semiconductor material (body link 32) which provides thermal conduction between respective bodies of said pair of transistors (col. 4, lines 60-67), but does not carry current during normal operation of said circuit stage. The body link does not carry current because it is an undoped region of silicon material (col. 5, lines 1-10). Intrinsic silicon is a poor conductor of electricity. In order for it to conduct, an extremely high voltage would have to be applied to the silicon. Such a voltage is too high for typical FETs and would thus destroy them. Therefore, during normal operation, the body link (32) does not carry current. Furthermore, the combination of the isolation oxide (40 in fig. 10B) and the body link (32) resist punch through between adjacent diffusions (col. 5, lines 53-65) and therefore act as a barrier or blocking region. An insulating material (69) totally surrounds at least part of said circuit stage.

In re claims 2 and 5, Flaker et al. does not specifically disclose that the circuit stage is an analog circuit stage. However, Flaker discloses that the invention is desirable in certain circuits such as differential amplifiers which are a type of analog circuit.

In re claim 6 (as far as understood), Flaker et al. shows (fig. 10B or 20) an integrated semiconductor-on-insulator circuit structure comprising a pair of transistors in a circuit stage which requires matched behavior of said pair (col. 7, lines 15-24). and a physical connection of metallic material which provides thermal conduction between respective bodies of said pair of transistors (col. 4, lines 60-67). Flaker et al. does not specifically disclose that the circuit stage is an analog circuit stage. However, Flaker discloses that the invention is desirable in certain circuits such as a differential amplifier which is a type of analog circuit. A physical connection of metallic material which provides thermal conduction between respective bodies of said pair of transistors is disclosed in an alternative embodiment in which metal may be used instead of the silicon body link to provide connection between the two transistor bodies (col. 6, line 53 – col. 7, line 4). An insulating layer (48) is beneath said pair and an insulating barrier (69) substantially surrounding said pair extends to said insulating layer.

In re claim 9, Flaker discloses (col. 7, lines 1-4) that said physical connection comprises metal interconnects between said transistors of said pair.

In re claim 16, Flaker et al. discloses a method of circuit operation, comprising the steps of providing a pair of matched transistors, in a circuit stage which requires matched behavior of said pair (col. 7, lines 15-24) and providing a physical connection of material which provides thermal conduction between respective bodies of said pair of transistors (col. 7, lines 5-14) and surrounding said circuit stage with an insulating material (col. 6, lines 35-53).

In re claim 17, Flaker et al. discloses (col. 7, lines 5-14) that said physical connection is of a semiconductor material.

In re claim 18, Flaker et al. does not specifically disclose that the circuit stage is an analog circuit stage. However, Flaker discloses that the invention is desirable in certain circuits such as a differential amplifier which is a type of analog circuit.

In re claim 19, Flaker does not specifically state that said physical connection does not carry current during normal operation of said circuit stage. Flaker implies that the body link does not carry current because it is an undoped region of silicon material (col. 5, lines 1-10). Intrinsic silicon is a poor conductor of electricity. In order for it to conduct, an extremely high voltage would have to be applied to the silicon. Such a voltage is too high for typical FETs and would thus destroy them. Therefore, during normal operation, the body link (32) does not carry current. Furthermore, the combination of the isolation oxide (40 in fig. 10B) and the body link (32) resist punch through between adjacent diffusions (col. 5, lines 53-65) and therefore act as a barrier or blocking region.

Claims 10-15, as far as understood are rejected under 35 U.S.C. 102(a) as being anticipated by Houston et al. (US 6,037,808).

In re claim 10 (as far as understood), Houston et al. shows (figs. 5a – 5d) an integrated semiconductor-on-insulator circuit structure, comprising a plurality of matched transistors in an analog circuit stage which requires matched behavior of said transistors (col. 9, lines 1-18) wherein respective bodies of said transistors are formed

from different semiconductor sections (sections of transistors T4 and T5 in figs. 5a), said sections being formed on an insulating layer (Ox) and at least partially separated by insulating material (see hash marks between sections of T4 and T5 in fig. 5a). The bodies are thermally coupled by a connection of non-insulating material (P-type body tie region BT in fig. 5a). Additionally, Houston discloses (col. 9, lines 8-18) that it is beneficial to not tie a potential to the bodies of the transistor.

In re claims 11 and 13, Houston discloses (col. 9, lines 35-43) that the bodies are electrically coupled by a connection of non-insulating material (P-type semiconductor body tie region BT in fig. 5a).

In re claim 12, 14, and 15, Houston discloses (col. 17, lines 20-37) that the invention is used in an analog circuit stage which comprises a current mirror. The stage is a matched pair of current-sourcing P-channel transistors since figure 5a shows that the source/drain regions are n-type and the channel is p-type for both transistors T4 and T5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flaker et al. (US 6,133,608) as applied to claims 1 and 6 above, and further in view of Houston et al. (6,037,808).

In re claims 3, 7, and 8, Flaker et al. shows all of the elements of the claims except the circuit stage being transistors in a current mirror. Flaker discloses that the invention having the body link is beneficial in differential amplifiers. Houston discloses (col. 17, lines 20-37) that a body tie is used in an analog circuit stage which comprises a differential amplifier having a current mirror. The stage is a matched pair of current-sourcing P-channel transistors since figure 5a shows that the source/drain regions are n-type and the channel is p-type for both transistors T4 and T5). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the matched transistor pair of Flaker by incorporating a current mirror because Houston teaches that current mirrors may also benefit from transistor matched pairs that use body ties.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Flaker et al. (US 6,133,608) as applied to claim 1 and further in view of Barrett, Jr. et al. (US 6,087,894)

In re claim 4, Flaker et al. shows all of the elements of the claims except the circuit stage being a cascode pair. Barrett, Jr. et al. discloses (abstract) that cascode coupled transistors can be used in SOI technology. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify

the matched transistor pair of Flaker by incorporating a cascode pair of transistors because Barrett teaches that cascode pairs may be implemented in SOI technology.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dachtera et al. (US 6,624,459 B1) and Oowaki et al. (US 5,895,956) also disclose transistors with device matching techniques.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew E. Warren
Matthew E. Warren
January 22, 2004